AMENDMENTS TO THE CLAIMS

Claims 1 – 10. (Cancelled)

11. (Original) A computer controlled method for processing an order for programmable integrated circuits (ICs), comprising the steps of:

storing a plurality of configurations;

pulling specified volumes of un-programmed ICs from inventory in response to an order from a customer;

programming the specified volumes of ICs with a configuration selected by the customer; and

packing the programmed ICs for shipment.

12. (Original) The method according to claim 11, wherein the ICs comprise field programmable gate arrays (FPGAs) and the step of programming comprises the steps of:

attaching a memory device to the FPGAs; and

programming the FPGAs using the selected configuration stored in the memory device.

13. (Original) The method according to claim 11, wherein the ICs each comprise a field programmable gate array (FPGA) and a memory device connected to the FPGA co-resident in one package and the step of programming comprises the step of:

programming the memory device while it is connected to the FPGA; and

powering up the FPGA and the memory device in order that the memory device configures the FPGA.

14. (Original) The method according to claim 11, wherein the ICs each comprise a field programmable gate array (FPGA) and a memory device connected to the FPGA co-resident on a common die and the step of programming comprises the step of:

programming the memory device while it is connected to the FPGA; and

powering up the FPGA and the memory device in order that the memory device configures the FPGA.

15. (Original) The method according to claim 12, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

16. (Original) The method according to claim 13, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

17. (Original) The method according to claim 14, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

18. (Original) The method according to claim 14, wherein the memory device is an anti-fuse.

19. (Original) The method according to claim 11, further comprising the step of testing the programmed ICs.

20. (Original) The method according to claim 11, further comprising the step of labeling the programmed ICs to reflect the selected configuration.

21. (Original) The method according to claim 11, further comprising tracking sales of the volumes of ICs programmed using the specific configuration.

22. (Original) The method according to claim 11, wherein the selected configuration is developed by the customer.

23. (Original) The method according to claim 20, wherein the step of labeling comprises marking the programmed ICs with at least one of a customer name and a customer logo.

Claims 24 – 28. (Cancelled)

29. (Original) A system for processing an order for programmable integrated circuits (ICs), comprising:

means for storing a plurality of configurations;

means for pulling specified volumes of un-programmed ICs from inventory in response to an order from a customer;

means for programming the specified volumes of ICs with a configuration selected by the customer;

means for packing the programmed ICs for shipment; and

computerized means for controlling the means for pulling, programming, and packing.

30. (Original) The system according to claim 29, wherein the ICs include field programmable gate arrays (FPGA) and the means for programming comprises:

means for attaching a memory device to the FPGA and programming the FPGA using the selected configuration stored in the memory device.

31. (Original) The system according to claim 29, wherein the ICs each include a field programmable gate array (FPGA) and a memory device connected to the FPGA, the means for programming programs the memory device while it is connected to the FPGA, and the system further comprises:

means for powering up the FPGA and the memory device in order that the memory device configures the FPGA.

32. (Original) The system according to claim 29, wherein the ICs each include a field programmable gate array (FPGA) and a memory device connected to the FPGA co-resident on a common die, the means for programming programs the memory device while it is connected to the FPGA, and the system further comprises:

means for powering up the FPGA and the memory device in order that the memory device configures the FPGA.

33. (Original) The system according to claim 31, wherein the FPGA and the memory device are co-resident on a common die.

34. (Original) The system according to claim 30, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

35. (Original) The system according to claim 31, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

36. (Original) The system according to claim 32, wherein the memory device is selected from a group consisting of a programmable read only memory (PROM), NAND flash, NOR FLASH, erasable PROM, and electrically erasable PROM.

37. (Original) The system according to claim 32, wherein the memory device is an anti-fuse.

38. (Original) The system according to claim 29, further comprising means for testing the programmed ICs.

39. (Original) The system according to claim 29, further comprising means for labeling the programmed ICs to reflect the selected configuration.

40. (Original) The system according to claim 29, further comprising means for tracking sales of the volumes of ICs programmed using the specific configuration.

41. (Original) The system according to claim 29, wherein the selected configuration is developed by the customer.

42. (Original) The system according to claim 39, wherein the means for labeling comprises means for marking the programmed ICs with at least one of a customer name and a customer logo.